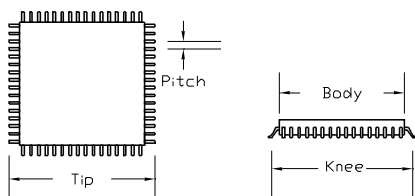# PA711D3-QD Data Sheet
44 pin QFP socket/40 pin DIP 0.6" plug

Supported Device/Footprints

Using this adapter, the Motorola 68HC711D3 in the QFP package can be programmed on 40 pin DIP programmers.

Device			Footprint	
Mfgr	Device	Package	Device	Plug
Motorola	68HC711D3	QFP	68HC711E9	40 pin DIP

The QFP socket accepts packages with the dimensions listed below:

Body	Knee	Tip	Pitch
10.0 mm typical	11.0 mm typical	12 mm typical	0.8 mm
	11.6 maximum	13.2 maximum	

Adapter Construction

The adapter is made up of 3 sub-assemblies. They assemble via connectors making the adapter modular. This way the sub-assemblies can be replaced when they wear out.

When disassembling the adapter take care not to bend the pins. When reassembling the adapter note the pin 1 indicators to align the parts correctly.

Test Socket
QFP test socket:
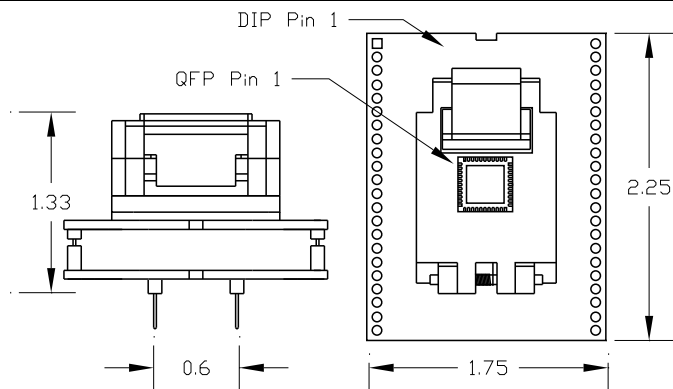   Enplas Part #: FPQ-44-0.8-06T   LSC Part #: 44QF-06T

44QFP-6T
Accepts the test socket and connects to the bottom board.

711D3-40
Performs the wiring shown in the Adapter Wiring section

Adapter Dimensions

Adapter Wiring

The following chart shows the connections from the QFP device to the adapter's DIP plug.

DEVICE	SIGNAL	PLUG
1	Gnd	6
2	Gnd	7
3	A6	8
4	A7	9
5	Vpp	10
6	D7	11
7	D6	12
8	Reset	13
9	CE-	14
10	D0	15
11	D1	16
12	D2	17
13	D3	18
14	D4	19
15	D5	20
16	Vcc	21
17	Gnd	22
18	N/C	-
19	N/C	23
20	N/C	-
21	Gnd	24
22	Gnd	25
23	Gnd	26
24	Gnd	27
25	N/C	-
26	OE-	28
27	Gnd	29
28	Gnd	30
29	A12	31
30	A11	32
31	A10	33
32	A9	34
33	A8	35
34	MODB	36
35	MODA	37
36	N/C	38
37	EXTAL	39
38	XTAL	40
39	Gnd	-
40	Gnd	1
41	A0	2
42	A1	3
43	A2	4
44	A3	5

PROG Mode Compatibility

While PROG mode makes the 'D3 look like a 27C256, it is not a perfect emulation. If the EPROM programmer's algorithm does not accomodate the 'D3's requirements, programming errors will occur. In that case there are three solutions.

1.   A different programmer.
2.   The programmer's manufacturer could add or change
an   algorithm to accomodate the 'D3.
3.   The adapter may be returned for a refund.

The technical reason for this compatibility problem is that the 27C256 is a fully asynchronous device. Address and control signal inputs may change at any time.

The 'D3 is a synchronous device. It may be thought of as a 27C256 with internal address latches. The latches are updated when A0 or CE(OE on older die) changes. For example: if CE and OE are low and an address bit is changed a 27C256 would soon output the contents of a new address. The 'D3 would not. The 'D3 will not recognize the new address until the address latch is updated by a logic change at either A0 or the proper control signal (OE or CE).

Logical Systems has written a memo about this. It is intended to assist EPROM programmer manufacturers who wish to support the 68HC11 family. Copies are available, just ask for one.

EPROM Address Mapping

During normal operation the 4K bytes of EPROM in a 'D3 is accessed at addresses F000 through FFFF. In PROG MODE the same EPROM accessed by the programmer at addresses 0000 through 0FFF.

On the EPROM programmer, data for address F000 will have to be programmed into address 0000. When installed and run the 'D3 will fetch that byte from address F000.

The executable/load address translation may be made at compile/assemble time or during EPROM programming. Some assemblers and linkers provide a PHASE command to generate HEX files where the EPROM addresses and executable addresses are not the same. Most programmers either allow the HEX file to be loaded with an offset or the EPROM to be programmed from anywhere in the RAM. Either method will do.

In PROG MODE A12, A13, and A14 are don't cares. The programmer will access the same EPROM location in the 'D3 at addresses 0000, 1000, 2000, ... 7000. To prevent this from being a problem, limit the programming range to 0000 through 0FFF.