

PA-XAG3FC-PD(Z) Data Sheet (Ver B)

44 pin PLCC socket/40 pin DIP 0.6" plug

Supported Device/Footprints

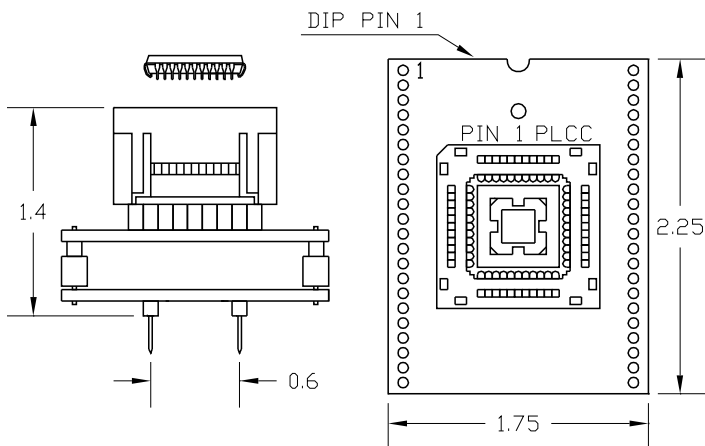
These adapters accept 44 pin PLCC and CLCC versions of the Philips 51-XAG3 and plug into an 87C51FC 40 pin DIP footprint.

Device		Footprint	
Manufacturer	Device	Device	Package
Philips	51XA-G3 PLCC	87C51FC	40 DIP 0.6"

There have been 3 versions of the XA-G3. Each version has slightly different programming requirements. These adapters support all 3 versions. The version are identified by their mask code. See the Jumper Settings section.

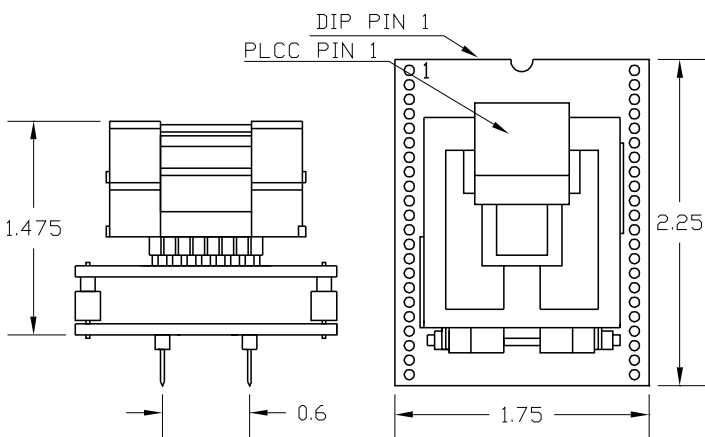
WARNING XSC6630 REQUIRES 10.75V VPP

Adapter Dimensions



Press rim to open socket, Press device to close

PA-XAG3FC-PD



PA-XAG3FC-PDZ

Memory Map

Both the 51XA-G3 and the 87C51FC (FC) contain 32K bytes of EPROM. Using the FC algorithm all of the 51XA-G3's EPROM (0000-7FFF) can be programmed.

Jumper Settings

There are two jumper blocks on the bottom board (XAG3-FC ver B). Set them according to the following chart to support the three known versions of the XA-G3 device. **The Mask Code is typically marked on the device's package.**

Mask Code	VPP	JP1	PSEN	JP2
XSC6389	12.75V	2-3	Low	X
XSC6503	12.75V	2-3	High pulse then Low	Open
XSC6630	10.75V	1-2	Low	X

X = Don't Care

JP1 controls a 2.0V step down. With pins 1-2 connected the stepdown is enabled.

JP2 isolates device PSEN from programmer PSEN. Leave it open.

Adapter Parts & Part Numbers

The following chart shows the various socket and board part numbers that make up these adapters.

Adapter	Test Socket	Top Board	Bottom Bd.
PA-XAG3FC-PD	44-106 or 44-306	44PL2-1 or 44PL2-3	XAG3-FC
PA-XAG3FC-PDZ	44-400	44PL2-Z	XAG3-FC

Adapter Construction

The adapter is made up of 3 sub-assemblies. They assemble via connectors making the adapter modular. This way the sub-assemblies can be replaced when they wear out.

When disassembling the adapter take care not to bend the pins. When reassembling the adapter note the pin 1 indicators to align the parts correctly.

Test Socket

PLCC Auto-Eject test socket:

Yamaichi Part #: IC120-0444-106

LSC #: 44-106

Yamaichi Part #: IC120-0444-306

LSC #: 44-306

ZIF Lidded socket:

Yamaichi Part #: IC51-0444-400

LSC #: 44-400

4PL2-1, -3, -Z

Accepts the test socket and connects to the bottom board.

XAG3-FC VerB

Performs the wiring shown in the Adapter Wiring section.

LOGICAL

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PA-XAG3FC-PD(Z) Data Sheet
Doc: XAG3FCPB.DOC
Rev 5/14/97
Page 1 of 2

Adapter Wiring

The following chart shows the connections from the PLCC device to the adapter's DIP plug.

Adapter Socket		Adapter Plug	
51XAG3-PLCC		87C51-FC-DIP	
Pin	Signal	Pin	Signal
1	VSS	20	VSS
2	P1.0	27	P2.6
3	P1.1	28	P2.7
4	P1.2	16	P3.6
5	P1.3	17	P3.7
6	P1.4	13	P3.3
7	P1.5	-	
8	P1.6	-	
9	P1.7	-	
10	RST*	20	VSS
11	P3.0	21	P2.0/A8
12	-	-	
13	P3.1	22	P2.1/A9
14	P3.2	23	P2.2/A10
15	P3.3	24	P2.3/A11
16	P3.4	25	P2.4/A12
17	P3.5	26	P2.5/A13
18	P3.6	14	P3.4/A14
19	P3.7	-	
20	XTAL2	18	XTAL2
21	XTAL1	19	XTAL1
22	VSS	20	VSS
23	VDD	40	VDD
24	P2.0	1	P1.0/A0
25	P2.1	2	P1.1/A1
26	P2.2	3	P1.2/A2
27	P2.3	4	P1.3/A3
28	P2.4	5	P1.4/A4
29	P2.5	6	P1.5/A5
30	P2.6	7	P1.6/A6
31	P2.7	8	P1.7/A7
32	PSEN* !!	29	PSEN*
33	ALE/PGM*	30	ALE/PGM*
34	-	-	
35	EA*/VPP !	31	EA*/VPP
36	P0.7	32	P0.7/D7
37	P0.6	33	P0.6/D6
38	P0.5	34	P0.5/D5
39	P0.4	35	P0.4/D4
40	P0.3	36	P0.3/D3
41	P0.2	37	P0.2/D2
42	P0.1	38	P0.1/D1
43	P0.0	39	P0.0/D0
44	VDD	40	VDD

! VPP has a voltage dropping circuit that is controlled by JP1. With pins 1-2 connected the 2.0V drop is enabled. With pins 2-3 connected, device pin 35 is connected to programmer pin 31.

!! The device's PSEN pin (pin 32) has a pulse generating circuit attached to it. With JP2 open the circuit generates a short pulse on the device's PSEN at power up. With JP2 shorted, the device and programmer PSEN signals are connected and the programmer controls the signal.

For all three versions JP2 should be left open.